

**SEMICONDUCTOR MEMORY DEVICE HAVING EXTERNALLY
CONTROLLABLE DATA INPUT AND OUTPUT MODE**

ABSTRACT OF THE DISCLOSURE

5 A semiconductor memory device having an externally controllable input and
output mode is provided. The semiconductor memory device includes a first and second
plurality of pads and an input and output mode set circuit electrically connected to the
first plurality of pads and the second plurality of pads, for generating a plurality of input
and output mode signals. The input and output mode set circuit cuts off signals received
10 from the first plurality of pads, controls the level of each of the input and output mode
signals to be at either a logic high level and a logic low level, and sets the input and
output mode when a voltage higher than the supply voltage of the semiconductor
memory device is applied to one of the second plurality of pads in a test mode. The high
voltage is not applied to the second plurality of pads and the input and output mode set
15 circuit controls the level of the input and output mode signals to be at either a logic high
level or a logic low level, and thus sets the semiconductor memory device to have one
input and output mode responsive to signals received from the plurality of pads, during a
normal operation. Accordingly, it is possible to externally change the input and output
mode of the semiconductor memory device.

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